

## Electrical Package Characterization

The success of today's high-speed digital and RF circuit designs highly depends on model and measurement accuracy including package characterization. Since the package operates in a complex electrical environment, accurate characterization requires a multi-level approach. Amkor's approach consists of a mix of electrical models based on 2-D/3-D and Full Wave 3-D package simulations in addition to time and frequency domain measurements. 2-D simulation and measurement based design guidelines are used for pre-layout feasibility and layout design rule generation whereas 3-D lumped, Full Wave 3-D and measurements are reserved for post-layout performance characterization and verification to ensure the design meets electrical specifications.

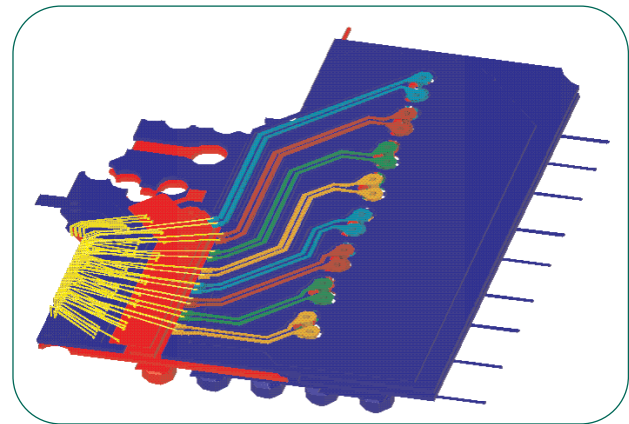
## Electrical Package Co-design and Optimization:

As the data transfer rate, gate counts and circuit density continue to grow, the impact of package electrical performance on overall system performance is growing. Today, delivering an optimum package requires more than just a robust layout and post-layout electrical simulation; it requires close interaction with our customers and substantial engineering support during layout phase. Amkor's Application Engineering and Characterization group closely works with the package designer to make sure the package layout meets all signal integrity performance specifications. You can trust Amkor to select and design the best package for your application and verify package electrical performance through state of the art simulation and measurement tools and techniques.

Amkor's Electrical Characterization Lab offers complete and accurate high frequency package characterization services. Amkor employs real time data acquisition either from a network analyzer or TDR (Time Domain Reflectometry) and uses a variety of high frequency EDA tools such as Agilent-ADS (Advanced Design System) and TDA Systems I-Connect to generate interconnect models based on measurement data.

## Modeling and Simulation Tools:

- Ansoft Maxwell Q3D & Q2D
- Ansoft Physical IC modeler (ParICs)
- Ansoft Synopsys Encore interface (AnsoftLinks)
- Ansoft Cadence APD interface (AnsoftLinks)
- Agilent ADS (Advanced Design System)
- Ansoft HFSS (High Frequency Structure Simulator)
- Optimal Corp. PakSi-E High Speed 3D Field Solver
- Agilent Momentum
- Agilent Picosecond Interconnect Modeling
- Synopsis HSpice and Awaves
- Cadence Advance Package Engineer (APE)
- Sigrity; Power SI and Speed2000
- TDA Systems I-Connect



Amkor's Application Engineering and Characterization group addresses the need for higher performance packaging through package co-design, measurement and simulation. To deliver an optimum design, Amkor utilizes measurement based design guidelines that have been developed over the years and extensive post-design modeling and measurements using state-of-the-art tools and techniques for verifications. We recognize that today's fast edges require careful design planning and attention to details. With Amkor's methodology, signal integrity issues such as risetime degradation, crosstalk, I/O bandwidth, power ground noise, time delay and ringing can be predicted before expensive prototypes are built.

VISIT AMKOR TECHNOLOGY ONLINE FOR LOCATIONS AND TO VIEW THE MOST CURRENT PRODUCT INFORMATION.

[www.amkor.com](http://www.amkor.com)



SS03E  
Rev Date: 06'04

## Electrical Package Characterization

Our customers are provided with the following data:

- Inductance (L) and mutual inductance ( $L_m$ )
- Capacitance (C) and mutual capacitance ( $C_m$ )
- Frequency dependent Resistance (R)
- S-parameter data in tabular and graphic format
- Smith charts
- Equivalent transmission line circuits
- Impedance (Z)
- Delay
- Spice decks
- IBIS models
- Power and ground voltage potential

### Measurement Equipment:

- Giga-Test Probe Station
- HP-8720D Network Analyzer (50 MHz-2020 GHz)
- HP-4285A Precision LCR Meter
- Tektronix TDS800 Digital Sampling Oscilloscope with 80E04 Differential TDR head



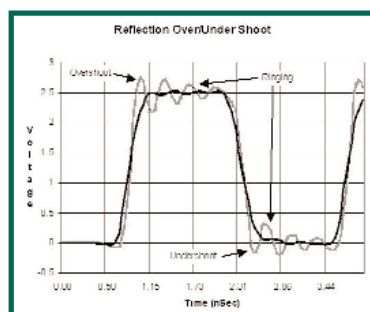
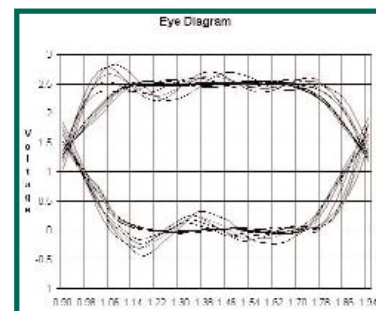
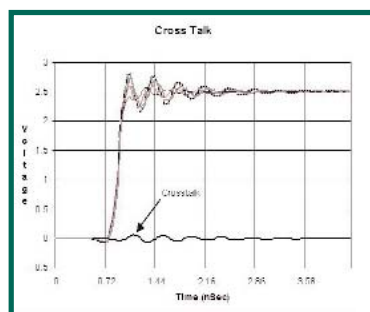
### Signal Integrity:

As signal rise times decrease and operating frequencies increase, signal fidelity becomes difficult to control. At Amkor, we have highly integrated signal integrity analysis capabilities to perform board/system level simulation. Packages are characterized with multiple signal integrity runs by varying the rise time, number of power/ground solder balls, number of simultaneously switching signals, etc. This provides our customers with the best-fit package for their customized Integrated Circuits. Signal degradation due to impedance mismatches, crosstalk, and simultaneous switching noise from the package can be evaluated and the package design can be modified to meet performance specifications. Amkor uses highly accurate 2-D/3-D-field

solvers and Cadence's Advanced APE for signal integrity analysis. The 3-D-field solver extracts resistance, capacitance and inductance in both lumped and distributed form to achieve the highest accuracy. Cadence's APE is used for delay optimization, crosstalk, reflection, impedance and 2-D parasitic extraction. Since Cadence's APE is tightly integrated with the layout tool, electrical rules can be passed to layout team before and during the design process restricting electrical rule design violations allowing for quicker design turnaround times.

### Signal Integrity Capability:

- Interface to most packaging CAD databases and DXF
- Generate propagation delay reports for entire net
- Perform SPICE simulations on individual nets in coupled and un-coupled analysis
- Perform cross talk, reflection, over/under shoot, and timing analysis
- Supply customers with package SPICE models for system level analysis
- Analyze and report skew timing between multiple drivers
- Analyze power ground bounce noise with 3-D extraction



VISIT AMKOR TECHNOLOGY ONLINE FOR LOCATIONS AND TO VIEW THE MOST CURRENT PRODUCT INFORMATION.

## Mechanical Package Characterization

### Interconnect Reliability:

Board level reliability is one of most important aspects of package selection. Electronic assemblies experience a variety of field use conditions during their life. Package-to-board interconnects are required to survive these conditions. As part of our strategy to provide complete packaging solutions to our customers, Amkor offers solder joint reliability characterization for all package styles.

### Temperature Cycle Tests:

Amkor employs the following three temperature cycle test conditions for board level reliability, depending on the intended end use application of the package. All of these conditions comply with IPC-9701 specifications.

In-situ electrical testing is performed to identify failures.



Condition	Min. Temp. (°C)	Max. Temp (°C)	Ramp Up Time (Minutes)	Ramp Down Time (Minutes)	High Temp. Dwell (Minutes)	Low Temp. Dwell (Minutes)	Cycle Duration (Minutes)
TC1	-40	125	15(+5/-0)	15(+5/-0)	15(+0/-5)	15(+0/-5)	60
TC2	-55	125	2 - 3	2 - 3	12 - 13	12 - 13	30
TC3	0	100	10(+2/-0)	10(+2/-0)	10(+0/-2)	10(+0/-2)	40

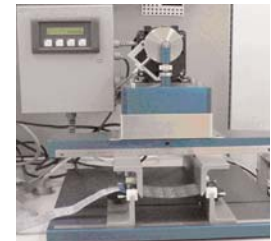
### Board Level Drop Test:

This test is implemented to provide a controlled environment to reproduce the interconnect failure mode commonly experienced during drop loading of handheld electronic systems (e.g., mobile phones, PDAs, etc.). Amkor took the lead in developing a board level drop test standard (JESD22-B111) and all tests are conducted as per this specification.



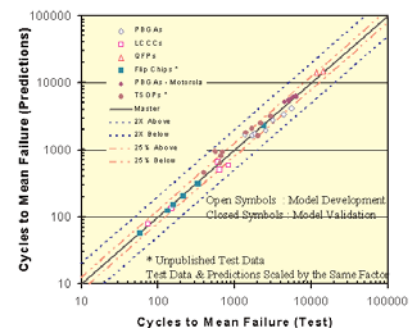
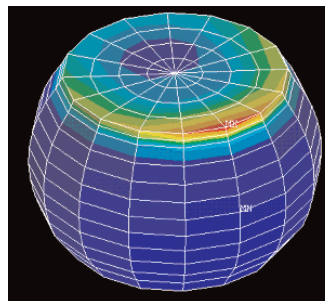
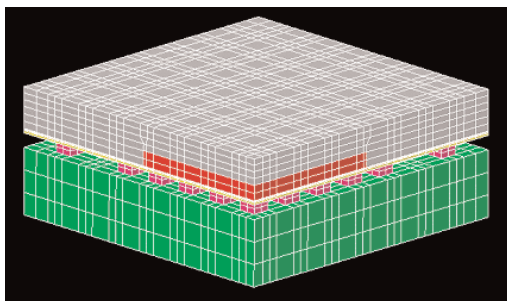
### Cyclic Bend Test:

The cyclic bend test consists of bending the printed circuit board assemblies using a 4-point bend test fixture. This test may be used to reproduce solder joint failures experienced in packages mounted on key pads.



### Board Level Solder Joint Reliability Prediction:

In addition to the above test capabilities, Amkor also offers solder joint life prediction capability using finite element simulation. The simulation provides a quick estimation of expected reliability and is used extensively in the pre-design stage. The life prediction approach correctly predicts the location of critical solder joint, location of failure (board or package side) with a high degree of accuracy for actual values.



In addition to temperature cycle condition simulation for Pb/Sn and lead-free solder, Amkor is developing simulation methodologies for bend and drop test simulations.

## Thermal Package Characterization

Amkor Technology offers advanced thermal test measurement capability and state-of-the-art modeling capabilities supporting all major electronic packaging styles.

### Amkor Proprietary Data Acquisition Software:

- Enhanced throughput and flexibility
- Automatic control and test capability
- Measure MCMs with up to 4 chips
- Heat spreader and heat sink analysis
- Perform system level measurements

### Wind Tunnel Facility:

Amkor's closed loop wind tunnel is capable of controlling airflow from 50 to 1600 LPM and air temperature from 18 °C to 65 °C. The tunnel spatial uniformity of velocity is  $\pm 1\%$  of the mean value. The test section is 12x12 inches with a contraction area of 6.5:1. Up to three boards can be tested simultaneously. A data acquisition and control system provides automated testing over a preset range of flow rate and power levels. Steady state convergence tests, based on die level temperature, are used before stepping to the next power/flow condition. Data are retrieved automatically and stored in an Access database filing system.



### Theta jc and Theta jb Facility:

Cold plate facilities are available for measuring Theta jc and Theta jb.

### Test Boards:

Amkor maintains a library of JEDEC standard leaded and array format 1SOP and 1S2P test boards. Custom board design capabilities are also available.

### Thermal Test Reports:

Amkor amassed over 100 thermal test reports covering a wide array of packages ranging from power application packages such as a PSOP3, leaded packages such as LQFP, exposed pad packages such as MLFs and array packages such as PBGA. Thermal data includes theta ja over a range of power levels at flow velocities from 0.0 to 2.5m/s. Psi jt, psi jb and theta jc data are available in many of the thermal reports.

### Quick Thermal Calculators:

Quick thermal calculators are available for many package styles. Immediate thermal resistance estimations are available using a Web interface.

### Parametric Models:

Turnkey thermal models are also available using Ansys' parametric modeling capabilities. Fewer geometrical details are considered but the models are fully automated. Typical accuracy is 90% or higher.

### Detailed Models:

Amkor employs advanced thermal modeling techniques using finite element analysis (FEA). A CAD-based modeling approach developed at Amkor has consistently shown a 95% accuracy level when compared against test data. Individual details such as traces, vias, solder balls, etc. are explicitly modeled.

### Custom Thermal Solutions:

Custom thermal solutions are available at Amkor to optimize component level designs. This may include laminate or leadframe design optimization, material property evaluation and board layout analyses.

### Computation Fluid Dynamic (CFD) Model:

CFD models are used to more closely predict package performance in custom environments. This includes local flow conditions, system packaging and thermal interaction between neighboring components.

### Compact Thermal Models:

Compact thermal models are available for predicting system level performance. They are developed to provide "boundary condition independent" peak die temperature predictions.